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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/850,357	WALDIE ET AL.	
	Examiner	Art Unit	
	Joseph Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- *Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.*
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). *Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).*

Status

1)☒ Responsive to communication(s) filed on *07 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/7/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8, 18, 21, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kahle et al., U.S. Patent 5,995,743, hereinafter referred to as "Kahle".

3. Referring to claim 1, Kahle teaches an emulation assist unit embedded in a processor system (See Fig. 2). Kahle teaches the emulation assist unit having a guest instruction queue, this is interpreted as an auxiliary instruction queue including a plurality of storage registers programmable with a set of instructions (See Fig. 3). Kahle discloses the emulation assist unit having various control means including a guest dispatch unit that governs the insertion of instructions of the instruction queue into an instruction execution stream of the processor system (See Fig. 3).

4. Referring to claim 2, Kahle teaches the use of signal "gdispc" (See Fig. 3) that the causes the dispatcher to insert the next instruction in the instruction stream. The instructions are ordered by a sequential fetcher, this is interpreted as a predetermined order (See Col. 10, lines 40-62).

5. Referring to claim 3, Kahle discloses the use of a sequential fetcher for the order of the instructions, this is interpreted as accessing them in addressable sequential order (See Col. 10, lines 52-57).

6. Referring to claim 4, Kahle teaches the dispatcher inserting the next instruction after the signal, this is interpreted as the access means accessing the instruction for the queue automatically in response to the execution signal (See Col. 10, lines 40-62).

7. Referring to claim 5, Kahle discloses the instruction being executed by native instructions of the processor, this is interpreted as accessing the instructions from the queue at a rate commensurate with the processor system clock (See Col. 2, lines 30-37).

8. Referring to claim 6, Kahle teaches the dispatcher inserting the next instruction after the signal, this is interpreted as gating the instruction accessed from the queue into an instruction pipeline of the processor system for execution (See Col. 10, lines 40-62).

9. Referring to claim 7, Kahle discloses the use of a current entry pointer (See Fig. 3 and Col. 8, lines 13-20). This is interpreted as a designated register that characterizes the set of instructions and governs the accessing of means.

10. Referring to claim 8, Kahle teaches the use of the "gdispc" signal, this is interpreted as controlling a program counter during the insertion of the instructions into the execution stream (See Fig. 3).

11. Referring to claim 18, Kahle discloses the instruction queue as part of the emulation assist unit which is connected to the MMU (main memory unit) and BIU (bus interface unit), this is interpreted as the queue being memory mapped as part of the memory space of the processor and queue being coupled to a bus of the processor system (See Fig. 2).

12. Referring to claim 21, Kahle discloses the instruction queue as part of the emulation assist unit which is connected to the MMU (main memory unit) and BIU (bus interface unit), this is interpreted as the queue being memory mapped as part of the memory space of the processor and queue being coupled to a bus of the processor system (See Fig. 2).

13. Referring to claim 22, Kahle teaches executing both normal instructions and emulating guest instructions, this is interpreted as two modes of operation (See Col. 2, lines 20-25).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 9-17, 19, and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle in view of Jaggar et al., U.S. Patent 6,321,329, hereinafter referred to as "Jaggar".

16. Referring to claim 9, Kahle teaches all the limitations (See rejection of claim 1) except for the instructions being received from an external host device through a host interface means. Jaggar teaches instructions loaded by a serial scan chain and coprocessor using the IEEE 1149.1 standard, this is interpreted as a host interface and receiving instructions from an external host (See Col. 2, lines 18-19, 35-40 and Col. 3, lines 57-58). It would have been obvious to combine the serial scan chain and coprocessor of Jaggar with the auxiliary queue of Kahle. This would have been obvious

to do because it allows the main processor to be left operating at its normal clock speed whilst instructions are loaded (See Jaggar, Col. 1, lines 63-65).

17. Referring to claim 10, Kahle and Jaggar disclose all the limitations (See rejection of claim 9) including the use of the coprocessor, this is interpreted as receiving the instructions from the host interface without interrupting the processing operations of the processing operations of the processor system (See Col. 2, lines 35-40).

18. Referring to claim 11, Kahle and Jaggar teach all the limitations (See rejection of claim 9) including instructions loaded by a serial scan chain using the IEEE 1149.1 JTAG standard (See Col. 2, lines 18-19, and Col. 3, lines 57-58).

19. Referring to claim 12, Kahle and Jaggar disclose all the limitations (See rejection of claim 9) including the use of a serial scan chain using the IEEE 1149.1 JTAG standard, this is interpreted as the host interface comprising a host peripheral interface (See Col. 2, lines 18-19, and Col. 3, lines 57-58).

20. Referring to claim 13, Kahle and Jaggar disclose all the limitations (See rejection of claim 12) including the use of a serial scan chain using the IEEE 1149.1 JTAG standard, this is interpreted wherein the host peripheral interface is selected from the a group comprising a serial peripheral interface and a parallel peripheral interface (See Col. 2, lines 18-19, and Col. 3, lines 57-58).

21. Referring to claim 14, Kahle and Jaggar teach all the limitations (See rejection of claim 9) including the instructions being debug instructions (See Col. 1, lines 6-9).

22. Referring to claim 15, Kahle and Jaggar teach all the limitations (See rejection of claim 14) including the use of JTAG that includes TDI (data in) and TDO (data out) and registers (See Col. 14, lines 35-38). This is interpreted as the control means including storage registers for temporarily storing data for and resulting from the execution of the debug instructions.

23. Referring to claim 16, Kahle and Jaggar disclose all the limitations (See rejection of claim 9) including the instructions being debug instructions, this is interpreted as instructions from the host device including instructions for transferring data between the host device and processor system (See Col. 1, lines 6-9).

24. Referring to claim 17, Kahle and Jaggar teach all the limitations (See rejection of claim 16) including the use of JTAG that includes TDI (data in) and TDO (data out) and registers (See Col. 14, lines 35-38). This is interpreted as the control means including storage registers for temporarily storing data for and resulting from the execution of the data transfer instructions.

25. Referring to claim 19, Kahle teaches all the limitations (See rejection of claim 18) except for the instructions being debug instructions. Jaggar teaches debug instructions loaded by a serial scan chain using the IEEE 1149.1 standard, (See Col. 1, lines 6-9, Col. 2, lines 18-19, and Col. 3, lines 57-58). It would have been obvious to combine the serial scan chain of Jaggar with the auxiliary queue of Kahle. This would have been obvious to do because it allows the main processor to be left operating at its normal clock speed whilst instructions are loaded (See Jaggar, Col. 1, lines 63-65).

26. Referring to claim 23, Kahle discloses all the limitations (See rejection of claim 1) except for the use of an event state detector for trigger the insertion of the instructions. Jaggar teaches debug instructions loaded by a serial scan chain using the IEEE 1149.1 standard, (See Col. 1, lines 6-9, Col. 2, lines 18-19, and Col. 3, lines 57-58). Jaggar also discloses the use of triggering (See Col. 2, lines 15-17). This would have been obvious to combine the serial scan chain of Jaggar with the auxiliary queue of Kahle. This would have been obvious to do because it allows the main processor to be left operating at its normal clock speed whilst instructions are loaded (See Jaggar, Col. 1, lines 63-65).

27. Referring to claim 24 and 25, Kahle and Jaggar teach all the limitations (See rejection of claim 23) including of the use of both breakpoints and watchpoints (See Jaggar, Col. 2, lines 15-17).

28. Referring to claim 26, Kahle teaches an emulation assist unit embedded in a processor system (See Fig. 2). Kahle teaches the emulation assist unit having a guest instruction queue, this is interpreted as an auxiliary instruction queue including a plurality of storage registers programmable with a set of instructions (See Fig. 3). Kahle discloses the emulation assist unit having various control means including a guest dispatch unit that governs the insertion of instructions of the instruction queue into an instruction execution stream of the processor system (See Fig. 3). Kahle also teaches discloses the instruction queue as part of the emulation assist unit which is connected to the MMU (main memory unit) and BIU (bus interface unit), this is interpreted as the queue being memory mapped as part of the memory space of the processor and queue being coupled to a bus of the processor system (See Fig. 2).

Kahle does not teach the apparatus being a debug apparatus. Jaggar teaches debug instructions loaded by a serial scan chain using the IEEE 1149.1 standard, (See Col. 1, lines 6-9, Col. 2, lines 18-19, and Col. 3, lines 57-58). It would have been obvious to combine the serial scan chain of Jaggar with the auxiliary queue of Kahle. This would have been obvious to do because it allows the main processor to be left operating at its normal clock speed whilst instructions are loaded (See Jaggar, Col. 1, lines 63-65).

29. Referring to claim 27, Kahle and Jaggar teach all the limitations (See rejection of claim 26), including instructions loaded by a serial scan chain using the IEEE 1149.1 JTAG standard, this is interpreted as including a communications interface for coupling

the control means with a host system external the processor system for directing the operations (See Col. 2, lines 18-19, and Col. 3, lines 57-58).

30. Referring to claim 28, Kahle and Jaggar teach all the limitations (See rejection of claim 27) including the use of JTAG that includes TDI (data in) and TDO (data out) and registers (See Col. 14, lines 35-38). This is interpreted as the control means including storage registers for temporarily storing data for and resulting from the execution of the debug instructions.

31. Referring to claim 29, Kahle and Jaggar teach all the limitations (See rejection of claim 26) including Jaggar teaches debug instructions loaded by a serial scan chain using the IEEE 1149.1 standard, (See Col. 1, lines 6-9, Col. 2, lines 18-19, and Col. 3, lines 57-58). Jaggar also discloses the use of triggering (See Col. 2, lines 15-17).

32. Referring to claim 30, Kahle and Jaggar teach all the limitations (See rejection of claim 26) including the use of JTAG that includes TDI (data in) and TDO (data out) and registers (See Col. 14, lines 35-38). This is interpreted as the control means including storage registers for temporarily storing data for and resulting from the execution of the debug instructions.

33. Claims 20 and 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle in view of Jaggar and Diab et al., U.S. Patent 6,236,872, hereinafter referred to as "Diab".

34. Referring to claim 20, Kahle teaches all the limitations (See rejection of claim 18) except for the instructions being serial boot loader instructions. Jaggar teaches instructions loaded by a serial scan chain using the IEEE 1149.1 standard, (See Col. 2, lines 18-19, and Col. 3, lines 57-58). Diab teaches the using a JTAG TAP line to transmit a boot loader (See Col. 39, lines 9-13). It would have been obvious to combine the serial scan chain of Jaggar and the boot loader of Diab with the auxiliary queue of Kahle. This would have been obvious to do because it allows the main processor to be left operating at its normal clock speed whilst instructions are loaded (See Jaggar, Col. 1, lines 63-65) and because it allows the processor to boot from program memory (See Diab, Col. 39, lines 9-13).

35. Referring to claim 47, Kahle teaches an emulation assist unit embedded in a processor system (See Fig. 2). Kahle teaches the emulation assist unit having a guest instruction queue, this is interpreted as an auxiliary instruction queue including a plurality of storage registers programmable with a set of instructions (See Fig. 3). Kahle discloses the emulation assist unit having various control means including a guest dispatch unit that governs the insertion of instructions of the instruction queue into an instruction execution stream of the processor system (See Fig. 3).

Kahle does not teach the instructions to act as an auxiliary boot loader and operating at power-up mode when power-up is detected. Jaggar teaches instructions loaded by a serial scan chain using the IEEE 1149.1 standard (See Col. 2, lines 18-19, and Col. 3, lines 57-58). Diab teaches the using a JTAG TAP line to transmit a boot loader (See Col. 39, lines 9-13). It would have been obvious to combine the serial scan chain of Jaggar and the boot loader of Diab with the auxiliary queue of Kahle. This would have been obvious to do because it allows the main processor to be left operating at its normal clock speed whilst instructions are loaded (See Jaggar, Col. 1, lines 63-65) and because it allows the processor to boot from program memory (See Diab, Col. 39, lines 9-13).

36. Referring to claim 48, Kahle, Jaggar, and Diab disclose all the limitations (See rejection of claim 47) including cache (See Kahle, Fig. 2). Kahle discloses the emulation assist unit having various control means including a guest dispatch unit that governs the insertion of instructions of the instruction queue into an instruction execution stream of the processor system, this is interpreted as cause a stream of instructions to be loaded into the cache (See Fig. 3). Jaggar teaches instructions loaded by a serial scan chain using the IEEE 1149.1 standard, this is interpreted as a communication interface to access instructions from an external system (See Col. 2, lines 18-19, and Col. 3, lines 57-58).

37. Referring to claim 49, Kahle, Jaggar and Diab teach all the limitations (See rejection of claim 48) including Kahle discloses the emulation assist unit having various control means including a guest dispatch unit that governs the insertion of instructions of the instruction queue into an instruction execution stream of the processor system, this is interpreted means for causing the execution of the instructions loaded into cache (See Fig. 3).

38. Referring to claim 50, Kahle teaches executing both normal instructions and emulating guest instructions, this is interpreted as the auxiliary queue being reconfigurable to another mode of operation (See Col. 2, lines 20-25).

39. Claims 31-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle in view of Mukherjee, U.S. Patent 6,757,881.

40. Referring to claim 31, Kahle teaches an emulation assist unit embedded in a processor system (See Fig. 2). Kahle teaches the emulation assist unit having a guest queue, this is interpreted as an auxiliary data queue including a plurality of storage registers programmable with a set of instructions (See Fig. 3). Kahle discloses the data queue as part of the emulation assist unit which is connected to the MMU (main memory unit) and BIU (bus interface unit), this is interpreted as the queue being memory mapped as part of the memory space of the processor and queue being

coupled to a bus of the processor system (See Fig. 2). Kahle discloses the emulation assist unit having various control means (See Fig. 3).

Kahle does not teach the register being fabricated to survive an upset transient. Also Kahle does not disclose a monitoring means for detecting an onset of the upset transient. Mukherjee teaches detecting faults from cosmic radiation in registers (See Col. 2, lines 50-60). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the auxiliary queue system of Kahle with the detection and of faults or upset transients caused by cosmic radiation of Mukherjee. This would be obvious to one of ordinary skill in the art at the time of the invention to do because it an economically feasible way to provide electronics to detect and recover (See Col. 1, lines 63-67).

41. Referring to claim 32, Kahle and Mukherjee disclose all the limitations (See rejection of claim 31) including the data being instructions of a program (See Kahle, Col. 2, lines 29-33).

42. Referring to claim 33, Kahle and Mukherjee teach all the limitations (See rejection of claim 32) including electronics detecting and recovering from the fault, this is interpreted as the control means governed by monitor means for program operation during the upset transient (See Mukherjee, Col. 1, lines 63-67).

43. Referring to claim 34, Kahle and Mukherjee disclose all the limitations (See rejection of claim 31) including a fault caused by cosmic radiation, this is interpreted as a high radiation upset transient (See Mukherjee, Col. 2, lines 50-52).

44. Referring to claim 35, Kahle and Mukherjee teach all the limitations (See rejection of claim 31) including a checker circuit that compares data, this is interpreted as majority voted registers (See Mukherjee, Col. 2, lines 11-12), and initiating a software or hardware recovery sequence, this is interpreted as powering down the systems external to the processor during the upset transient (See Mukherjee, Col. 2, lines 16-18).

45. Referring to claim 36, Kahle and Mukherjee teach all the limitations (See rejection of claim 35) including initiating a software or hardware recovery sequence, this is interpreted as restoring power and transferring data stored in the registers of the auxiliary data queue (See Mukherjee, Col. 2, lines 16-18).

46. Referring to claim 37, Kahle and Mukherjee teach all the limitations (See rejection of claim 31) including initiating a software or hardware recovery sequence, this is interpreted as restoring power and transferring data stored in the registers of the auxiliary data queue (See Mukherjee, Col. 2, lines 16-18).

47. Referring to claim 38, Kahle and Mukherjee teach all the limitations (See rejection of claim 31) including registers that contains data caused by the fault, this is interpreted as selected registers of the processor system represent a state thereof at the onset of the upset transient (See Mukherjee, Col. 2, lines 55-60).

48. Referring to claim 39, Kahle and Mukherjee disclose all the limitations (See rejection of claim 31) including Kahle discloses the emulation assist unit having various control means including a guest dispatch unit that governs the insertion of instructions of the queue into an instruction execution stream of the processor system (See Fig. 3).

49. Referring to claim 40, Kahle teaches an emulation assist unit embedded in a processor system (See Fig. 2). Kahle teaches the emulation assist unit having a guest queue, this is interpreted as an auxiliary data queue including a plurality of storage registers programmable with a set of instructions that store data (See Fig. 3).

Kahle does not teach the register being fabricated to survive an upset transient. Also Kahle does not disclose detecting an onset of the upset transient. Mukherjee teaches detecting faults from cosmic radiation in registers (See Col. 2, lines 50-60). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the auxiliary queue system of Kahle with the detection and of faults or upset transients caused by cosmic radiation of Mukherjee. This would be obvious to one of ordinary skill in the art at the time of the invention to do because it an economically feasible way to provide electronics to detect and recover (See Col. 1, lines 63-67).

50. Referring to claim 41, Kahle and Mukherjee disclose all the limitations (See rejection of claim 40) including a fault caused by cosmic radiation, this is interpreted as a high radiation upset transient (See Mukherjee, Col. 2, lines 50-52).

51. Referring to claim 42, Kahle and Mukherjee teach all the limitations (See rejection of claim 40) including a checker circuit that compares data, this is interpreted as majority voted registers (See Mukherjee, Col. 2, lines 11-12), and initiating a software or hardware recovery sequence, this is interpreted as powering down the systems external to the processor during the upset transient (See Mukherjee, Col. 2, lines 16-18).

52. Referring to claim 43, Kahle and Mukherjee teach all the limitations (See rejection of claim 42) including initiating a software or hardware recovery sequence, this is interpreted as restoring power and transferring data stored in the registers of the auxiliary data queue (See Mukherjee, Col. 2, lines 16-18).

53. Referring to claim 44, Kahle and Mukherjee teach all the limitations (See rejection of claim 40) including initiating a software or hardware recovery sequence, this is interpreted as restoring power and transferring data stored in the registers of the auxiliary data queue (See Mukherjee, Col. 2, lines 16-18).

54. Referring to claim 45, Kahle and Mukherjee teach all the limitations (See rejection of claim 40) including registers that contains data caused by the fault, this is interpreted as selected registers of the processor system represent a state thereof at the onset of the upset transient (See Mukherjee, Col. 2, lines 55-60).

55. Referring to claim 46, Kahle and Mukherjee disclose all the limitations (See rejection of claim 39) including Kahle discloses the emulation assist unit having various control means including a guest dispatch unit that governs the insertion of instructions of the queue into an instruction execution stream of the processor system (See Fig. 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. After approximately October 15, the examiner can be reached at the new Alexandria telephone number, (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
September 16, 2004

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